

**Attorney Docket No.: 100794-00109 (FUJA 18.905)**

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Inventor(s) : Susumu NIKAWA et al.  
Serial No. : 09/923,054  
Confirmation No. : 9863  
Filed : August 6, 2001  
Title : **POWER REDUCING APPARATUS ...**  
Examiner : Md S. Elahee  
Group Art Unit : 2614

December 17, 2007

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

**PRE-APPEAL BRIEF REQUEST FOR REVIEW**

SIR:

Applicants hereby petition for a two-month extension, a petition pursuant to 37 C.F.R. §1.136(a) and authorization to charge the requisite fee being enclosed.

In connection with the Pre-Appeal Brief Request for Review submitted herewith and in response to the final Office Action dated July 17, 2007, Applicants request a panel review to determine whether the Examiner has failed to properly establish bases for a § 103 rejection of pending claims 3-4 and 6-7 in the subject application. And, in support thereof, Applicants respectfully submit the following:

## **REMARKS**

Claims 1, 2, and 5 have been canceled. Claims 3-4 and 6-7 remain pending in this application.

Claims 3-4 and 6-7 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Applicants Admitted Prior Art (“AAPA”) in view of U.S. Patent No. 6,014,132 to Shimada et al. Applicants respectfully traverse the rejection.

The Examiner cited page 3, lines 5-7 in the specification as alleged AAPA on the claimed feature of maintaining an efficiency of a DC/DC converter at an optimum level in a predetermined low-power consumption mode. Such portion of the specification reads as follows:

“However, these two methods have had a problem in that the operation efficiency of the DC/DC converter of the power source unit 27 shown in Fig. 2 is lowered.”

Applicants pointed out that such description in alleged AAPA clearly only constituted Applicants’ own recognition of the very problem of inefficiency with prior art techniques that do not optimize DC/DC converter efficiency. And Applicants demonstrated that the cited description in the application is not AAPA disclosure of any known technique to maintain an efficiency of a DC/DC converter at an optimum level in a predetermined low-power consumption mode, as claimed. Plainly, such cited portion of the specification only describes prior art DC/DC converter suffering the disadvantage of having operation efficiency being lowered.

In response, the Examiner maintained the rejection in the final Office Action by arguing that this cited language from the specification describes a lowered efficiency level that still may be considered an “optimum” level at particular power levels, as claimed.

Applicants, again, respectfully point out that the cited portions of AAPA do not disclose or suggest ***maintaining*** efficiency at any level. The statement, again, constitutes

only Applicants' own recognition of a disadvantage in prior art techniques, and therefore, does not constitute an admission of any prior technique maintaining an efficiency at any level. In particular, Applicants refer to Fig. 8 of the application, which clearly illustrates prior art techniques having lowered and decreasing efficiency, and the cited portions of the specification do not include any disclosure or suggestion that the efficiency would be maintained at any lowered level. Applicants, therefore, respectfully submit that the alleged AAPA does not disclose or suggest the claimed feature of "determining a switching clock frequency of the DC/DC converter to maintain an efficiency of the DC/DC converter at an optimum level in the display color number limiting mode," for which the Examiner relied upon such alleged AAPA in the § 103 claim rejection. (Emphasis added)

The Examiner conceded that

"Applicant[s'] admitted prior art does not teach the following limitation:  
'determining one of the plurality of switching clock frequencies to maintain an efficiency of the DC/DC converter' and 'switching the frequency to the determined switching clock frequency, and operating the DC/DC converter at this frequency,'"

and cited and relied upon Shimada et al. as a combining reference that allegedly suggests these features. Page 4, lines 13 et seq. of the Office Action. Applicants demonstrated in the previous Response to Office Action that the cited portions of Shimada et al. only include description of a CPU clock frequency being reduced to reduce the power consumption of the CPU during a "standby mode." And Applicants demonstrated that such portions of Shimada et al. do not include any description on the operating efficiency of the CPU during such a "standby mode"—which would actually suggest a non-operation of the CPU—and, thus, also fail to disclose or suggest determining a switching clock frequency of a DC/DC converter to maintain an efficiency of the DC/DC converter at an optimum level.

In response, the Examiner did not substantively address Applicants' arguments but merely contended that Applicants' "argument [with respect to Shimada et al. were] irrelevant because, the examiner did not rely upon **Shimada** to teach the limitation." Page 3, lines 1-2 of the Office Action. But as cited above, the Examiner clearly relied upon Shimada et al. as a combining reference in the manner addressed by Applicants. Indeed, the Examiner stated, on page 4, lines 17-20 of the very same Office Action,

“**Shimada** teaches determining one of the plurality of switching clock frequencies to maintain an efficiency of the battery [i.e., DC/DC converter] and switching the frequency to the determined switching clock frequency, and operating the DC/DC converter at this frequency...”

such arguments being taken verbatim from the previous Office Action. Thus, Applicants directly and substantively addressed the Examiner's rejection based on AAPA and Shimada et al. by clearly pointing out and demonstrating the shortcomings of the cited references, and, correspondingly, the proposed combination of references. Again, Applicants demonstrated that the cited portions of Shimada et al. do not include any description on the operating efficiency of a CPU during a “standby mode,” and, thus, also fail disclose or suggest determining a switching clock frequency of a DC/DC converter to maintain an efficiency of the DC/DC converter at an optimum level while a corresponding display unit is in a display color number limiting mode.

And again, even assuming, arguendo, that it would have been obvious to one skilled in the art at the time the claimed invention was made to combine AAPA and Shimada et al., such a combination would still have failed to disclose or suggest,

“[a] method of reducing power consumption of a portable terminal equipped with a display unit to which power is supplied from a DC/DC converter, the method comprising the steps of:

monitoring the display unit to see whether the display unit is in a display color number limiting mode or not;

determining a switching clock frequency of the DC/DC converter to maintain an efficiency of the DC/DC converter at an optimum level in the display color number limiting mode;  
and

switching the frequency to the determined switching clock frequency, and operating the DC/DC converter at this frequency,” as recited in independent claim 3. (Emphasis added)

Accordingly, Applicants respectfully submit that claim 3, together with claim 6 dependent therefrom, is patentable over AAPA and Shimada et al., separately and in combination, for at least the foregoing reasons. Claim 4 incorporates features that correspond to those of claim 3 cited above, and is, therefore, together with claim 7 dependent therefrom, patentable over the cited references for at least the same reasons.

Finally, the Examiner referred to a “**Jambhekar**’s invention” on page 5, line 5 of the Office Action but has not provided any notice of any cited reference with such a first-named inventor. Applicants, therefore, respectfully submit that the Examiner’s rejection was improper for at least this additional reason.

Any fee due with this paper may be charged to Deposit Account No. 50-1290.

Respectfully submitted,

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